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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,326	02/26/2004	Guenter Stenz	X-1478 US	3972

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,326	STENZ ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-12,14-22 and 24-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-12,14-22 and 24-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/29/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/787,326 filed on 2/26/2004. Claims 1-2, 4-12, 14-22 and 24-30 remain pending in the application, where claims 3, 13 and 23 are canceled.

Drawings

2. Drawing(s) filed on 26 February 2004 that has been accepted is now objected to. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 4-12, 14-22 and 24-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Singh et al. (6,779,169 B1).

5. As to claims 1, 11 and 21, Singh et al. teach substantially the same invention. Singh et al. teach a method and apparatus for placement of components onto programmable logic device (floorplanning). The method comprising determining initial size for logic region based on Les and ESBs required for components on the logic region; then the initial size of the logic region may reshaped in response to the constraints of any child and/or parent logic region of the logic region (Fig. 7; col. 5 lines 50-67). In addition, Singh et al. automatically sizing region, where the logic region is reshaped such that it fits within the logic region (col. 4 lines 10-21). This would means that when reshaping a plurality of shapes or set of shaped has been pre-computed and created; and a best match is selected to fit space or area available on a programmable logic device (PLD). The sizes of the logic regions may be determined by a user or by a sizing method. The placement of the logic regions on a programmable logic device may be determined the user or by a placement method (col. 7-67). The placement method finds initial feasible locations for the logic regions that serve as a starting point solution that will be iteratively optimized (col. 6 lines 7-25). This would mean that the placed logic regions that have sizes and shapes obtained by automatically sizing method have been selected and initially placed on the PLD. After the initial placement, a placement optimization based cost function is come into play in order to improve the placement utilizing simulating annealing (col. 7 lines 30-67; col. 8 lines 1-67; col. 9 lines 1-7). Since the automatic reshaping of the logic region is done and used for initial placement before optimization that utilizing simulating annealing based on a cost function, a

plurality of shapes or set of shapes obtained by the automatic sizing method are computed and determined before to annealing as claimed.

6. As to claims 2, 12 and 22, Singh et al. teach splitting modules into sub-modules, wherein at least one of the sub-modules consists of components of a same type (the size of logic regions is reshaped). The reshaped logic regions are splitted modules (sub-modules) (Figs. 5-6).

7. As to claims 4, 14 and 24, Singh et al. teach simulated annealing comprising assign modules and assigned shapes to locations on the programmable logic device (Figs. 5-6; col. 5 lines 26-50).

8. As to claims 5, 15 and 25, Singh et al. teach swapping locations of components (Fig. 9, SWAP 1, SWAP 2).

9. As to claims 6, 16 and 26, Singh et al. teach simulating annealing comprising using bipartite matching of individual components. Fig. 1 shows LAB representing a number of LEs; MEGALAB representing a number of LABs; OCTANT representing a number of MEGALABs; COLUMN representing a number of HALF; HALF representing a number of COLUMNs; and a CHIP (PLD) representing whole circuit design. As shown in the figure, individual components are matched components.

10. As to claims 7, 17 and 27, Singh et al. teach simulating annealing comprising identifying modules that share a timing critical path and moving identified modules closer to one another to satisfy timing constraint. Col. 7 lines 7-40 describes how identified logic regions that share a timing critical path and moving the identified modules closer to one another to satisfy timing constraints.

11. As to claims 8, 18 and 28, Singh et al. teach placement of components of a system onto programmable logic devices (PLDs) (see summary). A Field Programmable Gate Array is a common and known programmable logic device.

12. As to claims 9, 19 and 29, Fig. 1 shows each shape of a set of shapes associated with a module (logic region) has a minimum width and height of at least a width and height of a largest relatively placed module to be placed within that module (smallest size LEs to form LAB; LABs to form MEGALAB...).

13. As to claims 10, 20 and 30, Singh et al. teach generating a flat placement flow for the circuit design (initial placement by positioning components of a system onto a target device utilizing programmable logic devices); and a user is prompted to define a logic region that includes a subset of components of the system to be grouped together. A location is determined for the user defined region on the target device that allows the system to satisfy timing constraints. This placement method is performed utilizing simulated annealing to measure a quality for the placement (floorplan) (see summary; Figs. 7, 12-13).

14. Claims 1-2, 4-12, 14-22 and 24-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Hwang et al. (6,457,164 B1).

15. As to claims 1, 11 and 21, Hwang et al. teach a method for designing a programmable logic device (summary) comprising defining modules of a circuit design comprising components of a same type (implemented modules, SIMs; col. 6); prior to annealing the circuit design, determining a set of shapes associated with each module (a plurality of shapes for precomputed placements a given SIM; col. 7 lines 23-60); and

annealing the circuit design to determining a floorplan by, at least in part, selecting a different shapes from the set of shapes corresponding to at least one module and applying the selected shape to the at least one module, wherein each iteration of annealing the circuit design is evaluated according to evaluation of a cost function (col. 6, col. 7, lines 30-67; col. 10 lines 27-45; col. 24 lines 1-20).

16. As to claims 2, 12 and 22, Hwang et al. teach splitting modules into sub-modules, wherein at least one of the sub-modules consists of components of a same type (col. 5 lines 40-67, col. 6 lines 1-27).

17. As to claims 4, 14 and 24, Hwang et al. teach annealing comprising assigning modules and assigned shapes to locations on the programmable logic device (col. 6 lines 1-27; col. 7 lines 30-67; col. 8 lines 1-24; col 24 lines 1-20).

18. As to claims 5, 15 and 25, Hwang et al. teach swapping locations of component of a same type that have associated grid sites, swapping two modules in a sequence pair, and switching the shapes of a module from one shape in the set of shapes associated with that module to another (col. 22). Note that swapping or changing placements between pair of modules are common practice in floorplanning of IC design layout (col. 27 lines 27-67).

19. As to claims 6, 16 and 26, annealing using bipartite matching of individual components is common practice in placement optimization, therefore it must be used during annealing as taught Hwang (col. 23 lines 40-67; col. 24 lines 1-20).

20. As to claims 7, 17 and 27, Hwang et al. teach identifying modules that share a timing critical path (share resources) and moving identified closer to one another (col.

25-26). Moving modules closer to each is common practice in layout IC design in order to minimizing interconnection.

21. As to claims 8, 18 and 28, Hwang et al. programmable logic is a Field Programmable Gate Array (FPGA, summary).

22. As to claims 9, 19 and 29, Hwang et al. each shape of a set of shapes associated with a module has a minimum width and height of at least a width and height of a largest relatively placed macro to be placed within that module (col. 25 lines 32-67; col. 26 lines 5-67). Note that a module or SIM and sub-modules or sub-SIMs or child SIM include width and height, a minimum width and height as well.

23. As to claims 10, 20 and 30, Hwang et al. teach generating a flat placement flow for the circuit design and comparing the annealed circuit design with the flat placement flow to determine a measure of quality for the determined floorplan (col. 23 lines 40-67; col. 24 lines 1-67; col. 25 lines 1-67; col. 26 lines 1-21).

Remarks

24. Applicants argued that Singh et al. do not appear to teach prior to annealing, determining a set of shapes associated with each module. Examiner disagrees. Please see above rejection. In addition, Hwang et al. also teach creating a plurality of shapes for each module (see above rejection). Two other references also teach the claimed invention of creating a plurality of shapes for each module for placement optimization.

25. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

26. Note that applicant is requested to review pertinent references (6,817,005 and US 2005/0183055) that also teach the claimed invention.

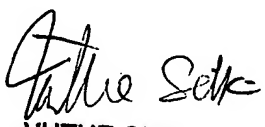
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek



VUTHE SIEK
PRIMARY EXAMINER